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The CDF Silicon Vertex Tracker ⋆

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Abstract

Real time pattern recognition is becoming a key issue in many position sensitive detector applications. The CDF collaboration is building SVT: a specialized electronic device designed to perform real time track reconstruction using the silicon vertex detector (SVX II). This will strongly improve the CDF capability of triggering on events containing b quarks, usually characterized by the presence of a secondary vertex.

SVT is designed to reconstruct in real time charged particles trajectories using data coming from the Silicon VerteX detector and the Central Outer Tracker drift chamber. The SVT architecture and algorithm have been specially tuned to minimize processing time without degrading parameter resolution.

Key words: Trigger; DAQ; Real Time Pattern Recognition; Silicon Detectors
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1 Introduction

Charged particle trajectory reconstruction is a very common task in HEP experiments. The history of HEP could be traced along the evolution of detectors and techniques employed to improve the resolution on track parameters. The typical processing time scale has evolved from months (in bubble chamber experiments) down to tenths and hundredths of second (in modern DAQ systems) in a non monotonic way.
The need for even faster tracking tools stems from two main issues:

- the fact that experiments are carried out to measure smaller and smaller cross sections. This means an increase in the event rate, as a consequence of improvements both in detectors and accelerators.
- the finer granularity of modern detectors, needed to achieve a good track resolution.

this means that experiments, especially those performed at hadronic colliders, are facing the need of more and more efficient triggering devices.
SVT has been designed as an high efficiency triggering device for events involving the production of long lived particles (like, for example, B meson production). The design has been constrained by the architecture of the whole CDF trigger, which requires SVT to process each event within $10\mu s$. A data driven pipelined architecture based on an asinchronous $630 Mb/s$ data path is the chosen solution. SVT is implemented on custom VME9U boards.

2 The CDF Framework

The Collider Detector at Fermilab CDF is a general purpose experiment for the study of $p\overline{p}$ collisions at a center of mass energy of $\sqrt{s} = 1.8 TeV$ at the Fermilab Tevatron collider. The collider and detector performance have evolved from 1985 to today, meeting and surpassing the design goals. The needs of more performing tools have led to the current detector and collider improvements, generally referred to as "Run II".
The Tevatron collider is planned to reach a luminosity of $2 \cdot 10^{32} cm^{-2} s^{-1}$, a minimum inter–bunch time of $132 ns$ with the mean number of overlapping events ranging between 2 and 6.
The CDF detector is concurrently being upgraded to exploit the full power

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of the new collider, with the goal of accumulating an integrated luminosity of $2fb^{-1}$.
The SVT project [1] is part of the effort of redesigning the trigger system to work at the increased event rate while improving and expanding the triggering capabilities.

2.1 Physics Motivation

B hadrons of sufficiently high transverse momentum are characterized by a large mean valued distribution of the impact parameter with respect to the beam axis. This means that events containing this kind of particles can be separated from non–long–lived background simply cutting on the track's impact parameter.
Tracking is in fact an essential ingredient for B physics studies, where long lived particles (the B meson travels about $450\mu m$ in the CDF environment) can be detected if a good enough tracking resolution is available. Up to now this resolution could only be efficiently achieved in the offline analysis, and was not fully exploited at trigger level.
One of the goals of CDF in Run II is to achieve online tracking resolution of the same order of magnitude as the offline; this might prove to be essential in order to be able to deal with the small ratio between the b-quark production cross section and the total inelastic $p\overline{p}$ cross section. Single track parameters (impact parameter in particular) are the most commonly used handles for the selection of b-flavoured events.
The ability to trigger on this kind of events will extend the sensitivity to new phenomena, broaden the inventory of heavy flavour decay channels and provide important control samples for top quark related measurements.

2.2 The CDF Tracking

The detector is described in detail elsewhere [2]. Here we will only outline the heart of the CDF tracking system: the COT and SVX II detectors.
The tracking systems are contained in a superconducting solenoid ($1.5m$ in radius and $4.8m$ in length) generating a $1.4T$ magnetic field parallel to the beam axis. In order to obtain a good resolution on the track parameters, two different detectors are used:

- The Central Outer Tracker (COT): a large open cell drift chamber designed to significantly outperform in response time its Run I predecessor (usually referred to as CTC)
- The Silicon VerteX detector (SVX II): a 5 layer silicon microstrip detector, placed near to the interaction region

The combined use of information from these detectors allows CDF to obtain an impact parameter resolution $\sigma_d \approx 30\mu m$. The new DAQ system has been designed to lower dead time as much as possible.

2.3 The CDF Trigger Structure

The whole CDF trigger and readout system is a three level pipelined deadtimeless device (with $5.5\mu s$ and $20\mu s$ latency time for the first two levels).
Each decision stage selects events on the basis of the data available at that stage of the pipeline: for example COT data is available at the earlier stage (Level 1) while the first SVX II information is available at Level 2.
A tracking engine for the COT (XFT, eXtremely Fast Tracker) is implemented at Level 1, while SVT is designed to exploit XFT's output and the SVX II data, thus working at Level 2.

2.4 SVT Resulting Constraints

Since we want to identify as many events as possible, SVT needs to be implemented as early as possible in the CDF pipeline. On the other hand SVT needs SVX II data to be available and thus can't be earlier than Level 2. The total Level 2 latency is $20\mu s$ on average, with $10\mu s$ reserved for the Level 2 processors, and thus about $10\mu s$ available for SVT processing. This defines the time constraints for SVT.
The resolution must be good enough to trigger on impact parameter and must therefore be of the same order of magnitude as the offline analysis.

3 The SVT Algorithm

To obtain a good enough resolution in a small enough amount of time we need a simple fitting algorithm that can be implemented directly in hardware as easily as possible.
The basic SVT architecture is that of an highly parallel data driven pipelined device. The algorithm implemented is conceived to distribute as much as possible the computational load in independent cascadeable stages. It is divided into a pattern recognition stage and a track fitting stage.
The pattern recognition stage is performed by the Associative Memory (AM) using a coarser special resolution. This is obtained by grouping silicon strips into wider *superstrips*. The AM identifies *roads* through the detector layers corresponding to combinations of *superstrips*, thus reducing combinatorics for

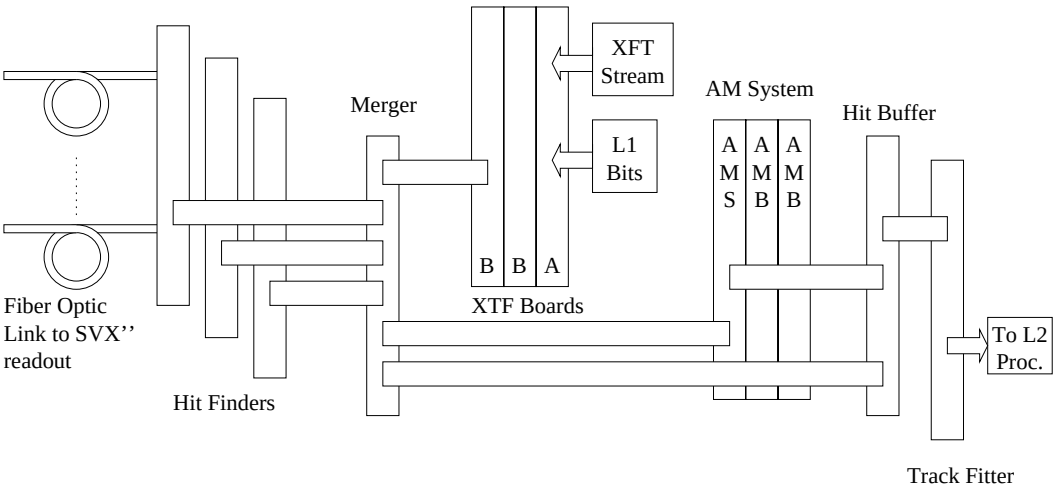

Fig. 1. Board organization of an SVT wedge (1/12 of the whole system).

the following fitting stage to combinations of hits contained in the same superstrip.
Typical superstrip size is $\approx 250\mu m$ while the detector resolution is typically one order of magnitude smaller. The fitting problem can be solved analytically, but the results are functional dependencies of the track parameters on the hit coordinates that can be extremely heavy even for a very performing CPU.
The SVT approach is to use a linear approximation: the linear approximation has been shown to be so good [1] that a single set of fitting constants can be used for each silicon detector mechanical wedge (30° in the detector azimuthal angle ϕ).
The combined use of pattern recognition and linearized fitting has been thoroughly simulated using Run I data [1], demonstrating the possibility of achieving offline resolution within the required time constraints. The trigger efficiency has also been studied on real Run I data samples, and found to be satisfactory.

4 Overall SVT architecture

The hardware implementation of the SVT algorithm solves both issues pointed out in 2.4.
SVT (see fig. 1) is organized as a set of 12 parallel engines, each processing the stream coming from one 30° SVX II wedge. Each SVT wedge consists of 9 VME9U boards, with data flowing from one board to the other through front panel data lines. The error monitoring is handled in parallel for pairs of SVT wedges by a supervising board (Spy Control).
Data flow from one board to the other is handled with the same uniform protocol for all the SVT elements; any SVT data port complying to this protocol is monitorable through a *Spy Buffer*, which is a circular buffer keeping a VME

accessible copy of the data flow. The Spy Control, together with the Spy Buffers thus acts as a sophisticated debugging tool for the SVT data streams: we can *freeze* the *spy–buffers* of all the SVT boards in coincidence with predefined events (error conditions) or under the supervision of an external program.

5 Single Board Functionality

The first processing stage in the SVT is performed by a set of three clustering boards (Hit Finders) for each SVT wedge. Each Hit Finder receives part of the SVX II output stream on 4 parallel high speed fiber optic links, applies a pedestal subtraction and a charge weighted clustering algorithm, and sends out *hit* coordinates.
The XFT output is processed in parallel with SVX II data and translated into an SVT stream by a set of three boards (1 XTFA and 2 XTFB) common to all 12 SVT wedges. The XTFA board receives the XFT stream, converts the relevant information into an SVT-like stream and sends it to the two XTFB boards through a custom backplane. The XTFB boards act each as a 6-fold fanout thus feeding 6×2 SVT wedges.
Hits from the three Hit Finders are merged together with the XFT output into a single stream by a Merger board. Data for the same event is output by the merger as soon as it is received, on two identical output streams.
The first *hit* stream goes to the Associative Memory Sequencer, which performs the pattern recognition stage of SVT together with 2 slave AM boards. Communication with the AM boards flows through a custom backplane. The AMS remaps hits into coarser *superstrips*, which are then fed through the backplane bus to 2×128 AM Chips, distributed on two AM boards.
Each AM chip is a full custom ASIC CMOS device [3] containing 128 roads, each road is defined as a combination of six superstrips, one for the XFT and 5 for the silicon layers. A road identifier is output back to the AMS through the backplane bus if the predefined set of superstrip coordinates for that specific road has been received. Matching *roads* start to flow back through the AMS to the output stream as soon as the last hit of the event has been received.
The second *hit* stream goes to the Hit Buffer, which receives also the *road* stream, combines each road with the corresponding hits and sends them to the Track Fitter.
The Track Fitter board loops on all possible *hit* combination within a given road, applying for each of them the linearized fitting algorithm. All the tracks falling within the preset χ^2 cut are then output and sent to the Level 2 processors.

6 Current Project Status

All the SVT boards have been designed and prototypes are currently being tested and finalized for production. Each prototype has been successfully tested up to the nominal 30MHz clock speed, and a mock–up of an SVT wedge (The "Vertical Slice Test") is being thoroughly tested at Fermilab.
The development of the software environment needed to handle such a powerful device is under way.
Board production will be started soon, and the whole system is planned to be installed before the first CDF II detector roll–in, scheduled for the year 2000.

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